MONOLITHIC CIRCUITS FOR 12 GHz DIRECT BROADCASTING SATELLITE RECEPTION

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ABSTRACT

This paper describes the design, fabrication and performances of gallium arsenide monolithic circuits of each of the principal microwave functions of a 12 GHz DBS receiver. The technology includes the use of Czochralski grown semi-insulating substrates, ion implanted active layers and localised growth of lines and interdigital capacitances. The low noise amplifier presents a 3,6 dB noise figure with 7,3 dB gain in the r.f. band. A dual gate mixer is presented with 6,5 dB noise figure and 2 dB conversion gain. The stable local oscillator has 32 mW output power and a stability of ± 0,3 ppm/K.

INTRODUCTION

A number of countries have recently indicated their intention to pursue their projects to launch 12 GHz direct broadcasting satellites in the mid 80's. Although exact system specifications may vary from country to country, the receiver requirements may generally be considered unchanged thus giving rise to the largest single market for microwave equipment to date. Although satisfactory hybrid front-ends already exist and are in advanced states of development[1], a number of research centres[2-4] are investigating the possibility of producing MMIC's for this application in view of the required large quantity production.

The advantages offered by the GaAs MESFET in fulfilling the principal roles in a downconverter have been described elsewhere[1, 5]. In order to render these functions monolithic, the necessary passive circuitry must be fully compatible with sub-micron gate FET processing and must be capable of reproductible results with a high yield.

This paper will outline the technology employed, the modelling of the lumped elements and give examples of monolithic MESFET subassemblies of each r.f. function ; 12 GHz low noise amplifiers, dual gate mixers and stable local oscillators designed to reply to the specifications of a DBS receiver.

LUMPED ELEMENTS

Detailed characterisation of the passive elements used to present the required impedances to the active components is fundamental to the design of MMICs. These elements include inductances (straight line, loop and spiral) and interdigital capacitances and their characterisation must include the element itself as well as its associated parasitic elements.

Inductances

An inductive line can be considered as a lumped element under certain conditions. Consider the normalised impedance at the input of a line loaded by z'

$$z = \frac{z' + j \tan \beta l}{1 + j z' \tan \beta l} \qquad (1)$$

when $z' \tan \beta l \ll 1$,

$$z = z' + j \beta l, \qquad (2)$$

that is the load impedance and a series inductance βl. Thus two conditions are necessary to consider the element as a lumped element : l must be small and z' must not be too high.

Another consideration is the equivalent inductance of the inductive term $j \beta l Z_o$,

$$L = Z_o \sqrt{\varepsilon_{eff}} \cdot \frac{1}{c} \qquad (3)$$

This term represents the inductance of a metal line in the presence of an earth plane at a distance h . This analysis is only valid for heights h less than h_{max} beyond which the equivalent inductance is greater than the lumped inductance of a line which is not perturbed by the presence of an earth plane. For typical line dimensions this maximum height would be about 300 microns thus severely restricting the application of a line model for substrates greater than this thickness.

Linear and loop inductances

A substrate thickness of 300 microns has been selected so as not to degrade the Q value of the lumped elements. Under these conditions the ground plane modifies only slightly the inductances and the following expressions remain valid[6].

$$L = 2\,l\,(2.3 \log_{10} (2\pi\, l/W) - 1 + W/l\pi) \qquad (4)$$

for a straight inductance and,

$$L = 12{,}57\,a\,(2.3 \log_{10} (8\pi\, a/W) - 2) \qquad (5)$$

for loop inductances,

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where a = mean radius in cms
W = line width in cms
l = line length in cms

Both straight and loop inductances have been characterized in reflection from 2 to 14 GHz. The results confirm the values of inductance in equations (4) and (5). Measurements carried out in transmission on identical elements enable the construction of an equivalent circuit for the inductance :

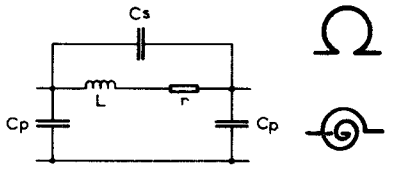


Fig. 1 : equivalent circuit of loop and spiral inductances

where C_s, C_p and r are the parasitic elements.

The Q value of a typical 1 nH inductance with a 20 micron track width and 3 micron metallisation thickness is approximately 25 at 10 GHz.

Spiral inductances

This element fulfils two rôles in our requirements ; that of matching element at frequencies around 1 GHz and that of r.f. choke for biasing.

Using a similar technique to that detailed above, equivalent circuits have been deduced for inductances whose values vary from 2 to 20 nH. Typically, the r.f. choke used in the oscillator circuit has 6 turns 10 micron track width and gap and a parallel resonant frequency at 12 GHz.

Interdigital capacitances

The interdigital capacitance for this type of periodic structure can be deduced from a closed form expression[7]. However, precise characterisation is required over a wide bandwidth in order to generate accurate estimations of the parasitic elements of the structure.

Measurements in reflection and in transmission have been effectuated from 2 to 14 GHz and the following equivalent circuits have been deduced, where L_s, L_p, C_p and r represent the parasitic elements.

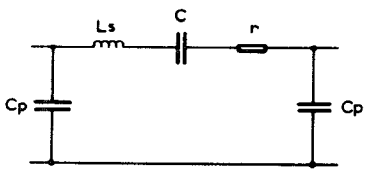


Fig. 2a : Equivalent circuit of interdigital series capacitances

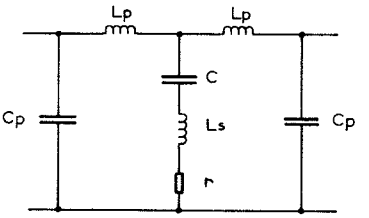


Fig. 2b : Equivalent circuit of interdigital parallel capacitances

Throughout circuit optimisation of the functions presented in this article, the complete equivalent circuit was used for each passive element in the matching circuits.

As a means of verifying the validity of the modelling of the lumped elements, a pass band filter was processed and designed to have more than 20 dB rejection in the image band of a 12 GHz receiver. The frequency response of this filter was sufficiently close to the predicted curve to conclude that the equivalent circuits were adequate for use in matching circuits.

CIRCUIT TECHNOLOGY

Two complementary technologies have been developed. The first, "semi-monolithic", involves the deposition of all necessary passive circuitry onto the gallium arsenide and subsequent bonding of the device into the circuit. This technology enables simple and rapid characterisation of the lumped elements and circuit optimisation. The second technology is purely monolithic and will be described in more detail.

The material used throughout this work is in-house Czochralski GaAs (resistivity $> 10^7$ ohm-cm) generating wafers of about 2" diameter. After crystallographic alignment the wafers are implanted, capped and annealed to produce uniform active layers. The wafers are then polished to a 300 µm thickness. This latter is chosen in order to maintain useful Q values of the passive elements.

The transistor technology is based on a self-aligned process[8] which produces gates of 0,7 micron lengths in a 2 micron drain-source spacing. Devices have gate widths of either 150 microns or 300 microns. The active areas are defined by a mesa etching isolation step down to the semi-insulating substrates onto which the circuit is grown by selective gold plating.

In order to minimise skin effect contributions and to generally increase the Q of the passive matching elements, a metallisation thickness of 3 microns was chosen. The processing that has been developed is based on selective growth through polyimide film and is capable of producing interdigital capacitances

with 5 micron gaps and 10 micron finger widths. The first step involves an evaporation of a continuous layer of Ti/Pt/Au on the GaAs, on the pads of the active components and the MIM capacitance contacts. Three microns of polyimide are then spun onto the wafer and polymerised after which the polyimide is capped, masked and plasma etched. Three microns of gold are then grown on the circuit pattern.

Finally, the remaining polyimide guide is removed by plasma etching and the adhesive layer of Ti/Pt/Au is removed by ion milling down to the semi-insulating GaAs substrate. Since the growth surface of the gold pattern remains constant throughout the process, the technique is controllable and has given reproducible interdigital capacitances with 5 micron interfinger gaps. (figure 3).

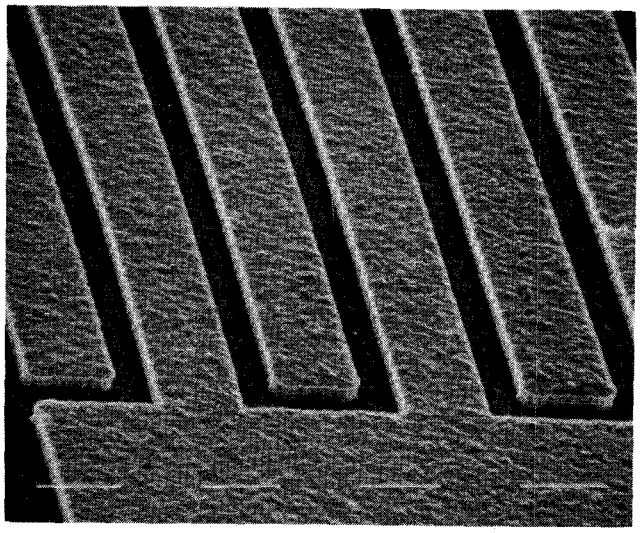


Fig. 3 : Interdigital capacitance : 10 micron finger width, 5 micron gaps.

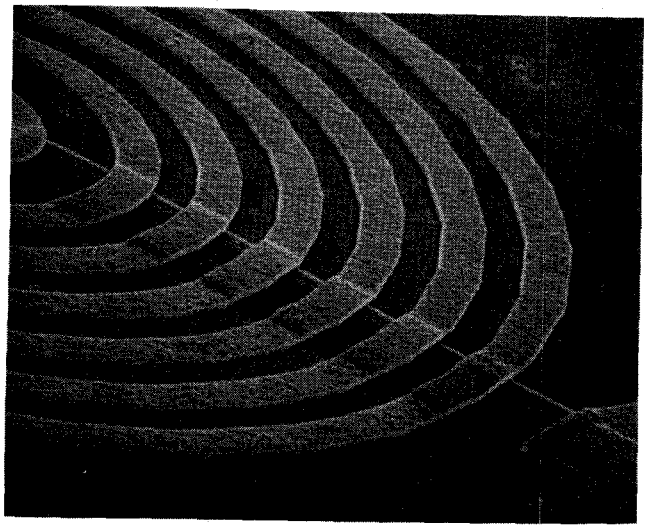


Fig. 4 : Spiral inductor and underpass interconnection : 10 micron track width, 10 micron gap.

Second level interconnections are necessary at a number of points in the circuits : between the source pads of the oscillator transistor, over the MIM capacitances and from the centre of the spiral inductances to the outside circuit. An example of this latter is shown in figure 4. This interconnection is an underpass beneath the turns of the inductor and is effectuated by using a negative photoresist that may subsequently removed to leave small air bridges.

MONOLITHIC SUB-ASSEMBLIES

Low noise amplifier

The noise figure of the downconverter is mainly fixed by that of the preamplifier and for that reason our target specification is a noise figure less than 4 dB with a gain of 7 dB per stage in the 11,7 - 12,5 GHz bandwidth.

In order to estimate an eventual dispersion in device parameters a number of ion implanted devices of the same geometry was characterised both in "S" parameters and in noise parameters. This characterisation was carried out using a "peeling" routine[9]. The measurements show typical dispersions of less than 5 % in amplitude and in phase for all four "S" parameters whereas the noise parameters present dispersions between 10 and 15 %.

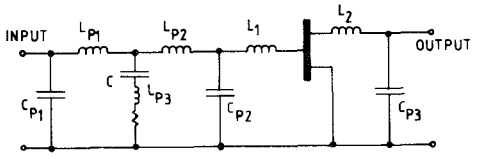
Resulting from this characterisation a number of amplifiers were designed using a maximum of two elements at the input and output of the device ; a configuration which is sufficient to cover the required bandwidth.

The conception of the amplifier was based on the analysis and characterisation of the lumped elements presented above. Care was taken in the use of inductive elements so as to use the equivalent electrical length of the element as a function of the impedance to be matched, particularly at the output of the device. Circuit optimisation was carried out both in noise and gain using COMPACT.

Amplifier performance

Both semi-monolithic and monolithic versions of these amplifiers were processed and measured between two coplanar lines in order to reduce access capacitances to the circuit. The ground contact was assured by a mesh down to the ground plane.

Under these conditions the best results for the single stage amplifier are a noise figure less than 3,6 dB and a gain more than 7,3 dB between 11,5 and 12,5 GHz (figure 5). VSWR is less than 1,9 at the input and less than 1,7 at the output. Figure 6 shows the circuit configuration of one of the amplifiers.



L_{pn}, C_{pn} are parasitic elements

Fig. 6 : Complete amplifier circuit topology.

Figure 7 shows the monolithic amplifier, the chip size is 1,6 mm^2.

Monolithic dual gate MESFET mixer

Single gate MESFET mixers have been successfully operated with as much as 6 dB conversion gain over octave I.F. bandwidths, however, their use in MMIC's is limited by their need for space consuming active or passive couplers for optimum operation. The dual gate MESFET provides an attractive alternative since the r.f. signal and the local oscillator frequencies can be applied to two separate gates and the intermediate frequency extracted from the drain circuit.

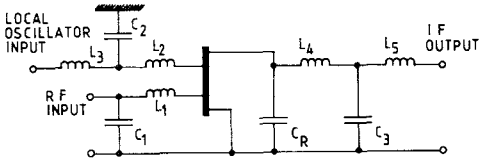
Optimum performance in terms of noise figure and stability occurs for bias points near pinch-off and by injecting the local oscillator modulation into the second gate with the signal injected into the first gate. Under these bias conditions non-linearities are provoked in the transconductances associated with both gates of the device, the effect being more pronounced in g_{m1} of the first gate. Furthermore there is a varistor-type modulation of the output conductance g_{d1} associated with the first gate.

Although optimisation of the performance of the device as a mixer by applying a non-linear, frequency domain analysis on each port is not yet completed, results of such an analysis on a single gate mixer[10] have been applied to the design of a dual gate mixer. These results indicated that optimum conversion gain was obtained with r.f. and local oscillator short circuits presented to the output of the mixer and an intermediate frequency short circuit presented at the input to the device. These conditions should be satisfied whilst maintaining power matching on the input at r.f. and local oscillator frequencies and i.f. matching at the output.

The totality of these conditions are difficult to fulfil in monolithic technology, however, an adequate r.f./local oscillator short at the mixer output can be obtained by using a parallel capacitance at its series resonant frequency directly at the drain terminal of the device. (C_R in figure 8).

This capacitance subsequently forms an integral part of the i.f. matching network at frequencies around 1 GHz.

After characterisation of the dual gate devices, matching circuits are calculated based on typical device parameters in the bands 11,7 - 12,5 GHz on the first gate, 10,8 GHz in the second gate and the corresponding i.f. band on the drain. This operation and limiting the number of passive matching elements gives rise to the circuit of figure 8.



C_R presents a series resonance at 12GHz

Fig. 8 : Dual gate mixer circuit

An example of this type of mixer realised in monolithic form is shown in figure 9. Chip size is 2,4 x 1,4 mm^2.

Mixer performance

The mixer was characterised in a 50 ohms coplanar circuit. The local oscillator was fixed at 10,8 GHz and the drive to the mixer's second gate was about 11 dBm. The r.f. input match presented a VSWR better than 2 across a 2 GHz bandwidth centred at 11,8 GHz. The corresponding intermediate frequency VSWR is less than 3,5 across the band.

Noise figure and gain performances are summarized on figure 10. Noise figures of 6,5 dB have been measured associated with maximum conversion gains of 2 dB.

Monolithic stable local oscillator

The monolithic GaAs FET oscillators reported up to now[11, 12] were based on a common gate configuration with inductive series feedback. The circuit presented here is a common source FET oscillator with series capacitive feedback stabilised using a dielectric resonator (DRO). This type of circuit demonstrated superior performance for temperature stable oscillator application. Stabilisation is obtained connecting the dielectric resonator circuit to the gate terminal. The circuit is shown in fig. 11 and is designed for frequencies around 11 GHz.

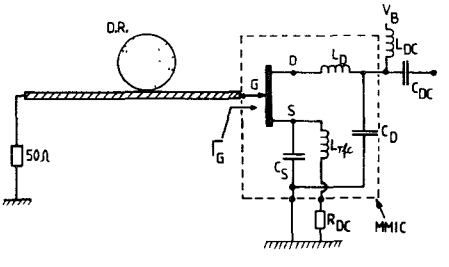


Fig. 11 : Complete stabilised monolithic oscillator topology

The FET has a 0,7 x 300 μm^2 gate. The source series feedback and the drain tuning circuit were determined on microstrip for an equivalent chip FET using an experimental oscillator design method : it consists in measuring the device line into the gate and optimizing the oscillator power ; calculated from the injected and reflected power at the gate and the power leaving the drain-port, following equations (6) and (7) :

$$P_{osc.} = P_D + P_i \left(|\Gamma|_G^{\,2} - 1\right) \qquad (6)$$

$$\Gamma_G = \Gamma_G (P_i) = \Gamma_R^{-1} \qquad (7)$$

where P_D and P_i are the drain power and injected gate power, Γ_G^i the reflexion coefficient at the gate ($|\Gamma|_G > 1$) and Γ_R the reflexion coefficient of the dielectric resonator stabilization circuit at the resonance frequency (fig. 11). The obtained impedances on the source and drain terminals were then synthesized using lumped elements and the design rules described in previous sections. The spiral bias inductance L_{rfc} is designed to present a maximum impedance (parallel resonance) at 11 GHz.

Oscillator performance

The monolithic oscillator chip shown in fig. 12 measures 1,2 x 1,4 mm^2. It has been tested in a 50 Ω microstrip test fixture. The performances of the monolithic oscillator, stabilized using a dielectric resonator, are given in table I. The output power can be linearly controlled by the bias supply from 0 to 26 mW.

Output power (V_{DS}= 4,9V)	32 mW (15 dBm)
Chip efficiency (V_{DS} = 4 V)	20 %
Frequency pushing (1,5 V $\leq V_{DS} \leq$ 5 V)	$\leq \pm$ 500 kHz
Frequency pulling (VSWR out = 3) (depends on coupling -factor β - of diel. resonators)	(a) < 20 MHz ($\beta \approx 10$)
	(b) < 1,5 MHz ($\beta \approx 4$)
Frequency stability (- 20°C ; 80°C)	< 1 ppm/K
Output power variation with temp.	< $\pm$ 0,75 dB

Table I : Performance of monolithic FET DRO

Temperature stabilization was obtained using a dielectric resonator which has a linear resonance frequency variation with temperature with a slope of around + 6 ppm/K and an unloaded Q factor of 1500 to 2000 ; it allows a better compensation of temperature drift of the active device parameters compared with nonlinear $f_r(T)$ characteristics (figure 13). This is a consequence of equation (8) that describes the oscillator's frequency drift with temperature[13].

$$S_o = S_R + \frac{\beta + 2}{4\,Q_r} \cdot S_D \qquad (8)$$

Here, $S_o = \frac{df}{fdt}$, $S_R = \frac{df_r}{f_r\,dT}$ and $S_D = \frac{\partial \phi_D}{\partial T}$

($\approx$ 2800 ppm/K) are the temperature drifts of oscillation frequency, resonance frequency of dielectric resonator and phase of the active circuit at the stabilization port, β and Q_r the coupling factor between the microstrip line and the resonator and the resonator's unloaded Q respectively.

CONCLUSIONS

MMICs have been developed which fulfil the requirements of the discrete sub-assemblies of a 12 GHz downconverter for domestic satellite reception. A summary of the analysis and characterisation of the lumped elements used in the circuit design is presented along with the technology used in their processing. Low noise amplifiers with 3,6 dB noise figure and 7,3 dB gain across the r.f. band, dual gate mixers with 6,5 dB noise figure and 2 dB conversion gains as well as stable local oscillators with 32 mW output power and stabilities of 1 ppm/K have been presented.

It is believed that the MMIC's presented in this article may form the basis for the complete monolithic integration of 12 GHz receivers.

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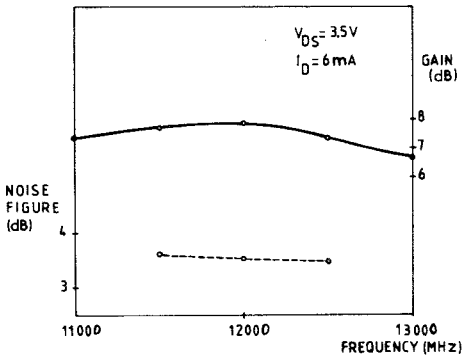

FIG. 5 : Gain and noise figure of single stage amplifier

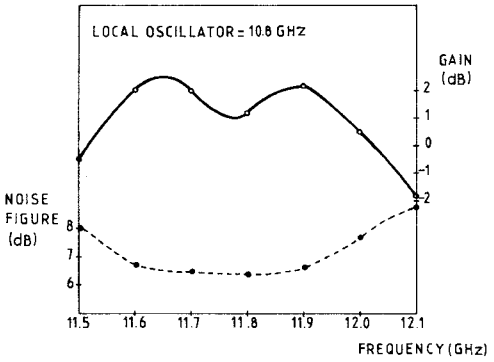

FIG. 10 : Mixer noise figure and conversion gain

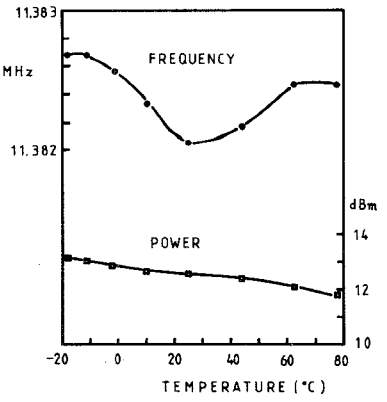

FIG. 13 : Temperature performance of stabilised monolithic oscillator

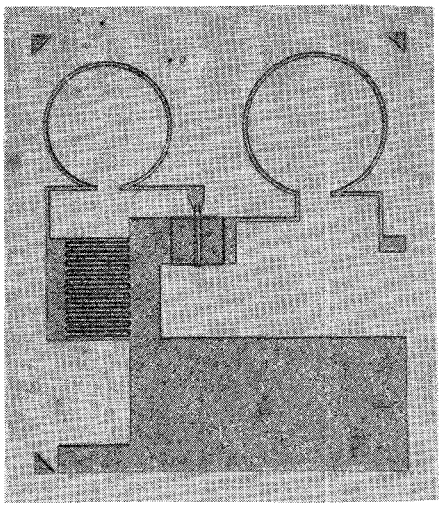

FIG. 7 : Monolithic one stage amplifier

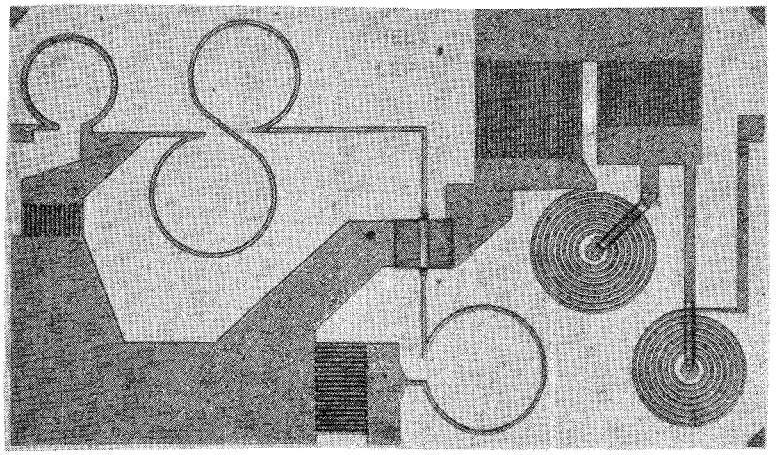

FIG. 9 : Monolithic dual gate mixer chip

FIG. 12 : Monolithic oscillator chip